TABLE OF CONTENTS

1.0 INTR	DDUCTION	1
1.1 DE	FINITION	1
	STORY	
1.3 LA	TCH-UP FUNDAMENTALS	2
	TCH-UP TEST METHODS	
	JEDEC JESD78 Style Tests	3
1.4.2	An Attempt at Transient Latch-up Test Method – ANSI ESD SP5.4-2008	
	(now ESD TR5.4-03-11)	
1.4.3	Panasonic "Machine Model" Transient Latch-up Method	5
2.0 LITEF	RATURE AND PREVIOUS WORK ON TLU	8
3.0 GENE	RAL OVERVIEW OF THE TLU PHENOMENON	9
3.1 IN	ERNAL TLU	9
3.1.1	Internal TLU during Supply Test (Overvoltage Stress)	11
3.1.2	Internal TLU during IO Test (Current Injection)	12
3.1.3	Internal TLU during ANSI/ESD SP5.4 (ESD TR5.4-03-11) Test	
	(Supply Undershoot)	14
3.1.4	Temperature Dependence in Internal TLU Phenomenon	15
3.2 Ex	TERNAL TLU	15
3.2.1	Trigger Pulse Slew-Rate in External TLU Phenomenon	17
3.2.2	Pulse Width Dependency in External TLU Phenomenon	20
3.2.3	External TLU Due to Bipolar Injection	22
3.2.4	Temperature Dependency in External TLU Phenomenon	22
4.0 APPL	ICATION AREAS	23
4.1 Did	GITAL AND HIGH-SPEED ICs (MICROPROCESSORS)	23
4.1.1	General Description of Possible TLU Threats in Digital and High-Speed ICs	23
4.1.2	Examples	23
4.1.3	Possible Test Methods to Reproduce these Examples	27
4.2 (W	IRELESS) COMMUNICATION	27
4.2.1	General Description of Possible TLU Threats in (Wireless) Communication	
	Applications	27
4.2.2	Examples	
4.2.3	Possible Test Methods to Reproduce these Examples	36
4.3 Au	TOMOTIVE	37
4.3.1	General Description of Possible TLU Threats in Automotive Applications	37
4.3.2	Examples	
4.3.3	Possible Test Methods to Reproduce these Examples	
4.4 Hi	GH-VOLTAGE APPLICATIONS (NON-AUTOMOTIVE)	
4.4.1	General Description of Possible TLU Threats in High-Voltage Applications	41
4.4.2	Examples	41

4.4.3	Possible Test Methods to Reproduce these Examples	47
4.5 L	ATCH-UP IN ANALOG DESIGN	48
4.5.1	Introduction	48
4.5.2	2 Examples	50
	Possible Test Methods to Reproduce these Examples	
	IMARY AND CONCLUSION	
5 1 C	ATEGORIES OF TLU FAILS AND TLU TESTS TO REPRODUCE THE FAILS	5 1
	ECOMMENDATIONS FOR NEXT STEPS TOWARDS STANDARDIZATION OF TLU TEST	54
	lethods	
6.0 BIBI	LIOGRAPHY	57
TABLES		
Table 1:	Timing Parameters of Voltage and Current Stresses	
Table 2:	Parameters for ESD TR5.4-03-11 (ANSI/ESD SP5.4-2008) Stress Pulse	
Table 3: Table 4:	Summary Table of MM TLU Pin / Power Supply Requirements and Failure Criteria. Compilation of Possible Test Methods to Reproduce the Examples Discussed in	8
Table 4.	Section 4.1.2	27
Table 5:	Latch-up Withstand Currents of Different Trigger Pulses (Static LU, Transient LU,	
	and CDE) at 100 °C	36
Table 6:	Compilation of Possible Test Methods to Reproduce the Examples Discussed in Section 4.2.2	37
Table 7:		07
	Section 4.3.2	40
Table 8:		47
Table 9	Section 4.4.2 Compilation of Possible Test Methods to Reproduce the Examples Discussed in	47
	Section 4.5.2	54
FIGURES	3	
Figure 1:		
- : 4	Substrate and Well Resistances	
Figure 1:	IV Curve of a Latch-up Showing Normal Low Current and Latch-up States	
Figure 3:	Transient Latch-up Pulse from ESD TR5.4-03-11 (ANSI/ESD SP5.4-2008)	
Figure 4: Figure 5:	MM TLU Test Setup Diagram ESD Test System / Power Supply / Oscilloscope Setup for MM Transient Latch-up	
Figure 6:	Equivalent Circuit of an Example ESD Power-Clamp Which is Sensitive to Certain	0
Ū	Slew-Rate	11
Figure 7:	IV of Power-Clamp from Figure 6, Comparison of TLP (dV/dt < 0.1 volts/ns) to	40
C: 0.	DC (dV/dt > 1 volts/µs)	
Figure 8: Figure 9:	Cross-Section of a Typical CMOS Output Driver Stage	12
i iguite 3.	in CMOS Technology	13
Figure 10	: TLU Trigger Current versus Pulse Width for a Typical Parasitic SCR in CMOS	13
	Technology	14
Figure 11	: Cross-Section of Two Inverters at Different Supply Voltage VDD1 and VDD2	
Figure 12	: Cross Section of an Arbitrary Region of the IC Containing a Critical Parasitic	
-	SCR, GR, and Injection Source	16
Figure 13	: Equivalent Circuit of the DC/DC Converter Which Contains an External Coil	17

Figure 14:	Voltage Drop at the Parasitic SCR during the External TLU Current Injection to the <i>n</i> + Diffusion	18
Figure 15:	Topology of the IO Test Chip Which was used for the TLU Tests, a Negative TLU Injection was Performed to the IO7, TLU Occurred at VDDP	
Figure 16	TLU Trigger Current of Two Samples (#42, #49) at IO7 versus: a) Pulse Fall	
. iguio io.	Time, Rising Edge was Kept at 10 µs; b) Pulse Rise Time, Falling Edge was	
	Kept at 10 µs	19
Figure 17:	External TLU Trigger Current versus Trigger Pulse Width [10] for Negative	
ga. e		20
Figure 18:	External TLU Trigger Current versus Trigger Pulse Width [8] for Positive	
	Current Injection to <i>p</i> +/ <i>n</i> - <i>well</i> Diode	21
Figure 19:	External TLU Trigger Current in Different Temperatures	
	Schematic of Power Array and ESD Clamp; Layout of Power Array and ESD	
9	Clamp	23
Figure 21:	10 ns TLP Characteristics Comparison between Stand-Alone ESD Clamp and	
J	ESD Clamp with Gate (Vin) Bias Variation	24
Figure 22:	Different Power-Rail ESD Clamp Circuits Designed with (A) Typical RC-Based	
Ü	Detection, (B) NMOS and PMOS Feedback, (C) PMOS Feedback, and (D)	
	Cascaded PMOS Feedback	25
Figure 23:	Measured VDD and IDD Waveforms on the Power-Rail ESD Clamp Circuit with	
J	NMOS and PMOS Feedback under System-Level ESD Test with ESD Voltage of	
	- 200 Volts	25
Figure 24:	Measurement Set-up of the System-Level ESD Test with Indirect Contact-	
	Discharge Test Mode	26
Figure 25:	Measured VDD Transient Waveform of One (CMOS IC #1) of the CMOS ICs	
	Inside the EUT with an ESD Voltage of -1000 Volts Zapping on the HCP	26
Figure 26:	Modified Component-Level TLU Measurement Set-up with Bipolar Trigger	26
Figure 27:	DC /V Characteristics of the Diode Triggered SCR Power Clamp	28
	EMMI Snapshot of the Power Clamp after EOS Stress	
	Part of the Core Circuitry Which has Involved Sensitive Parasitic SCR	29
Figure 30:	Topology of the External Connection Which Revealed Susceptibility to TLU, but	
	Could not Produce LU during the Standard JEDEC LU Test	30
Figure 31:	EMMI Snapshot of the Parasitic Thyristor after the Displacement Current	
	Injection through the CAP at Plug	
	ESD Protection Scheme of the USB Pad	
	Layout of the IO Pad and ESD Devices	
	Measurement at IO with Connected VDD 2.8 Volts	
	Measurement at IO with Disconnected VDD 2.8 Volts	32
Figure 36:	After the Injection of - 40 milliamperes (Pulse Width = 10 ms), the Current is	
	Observed at VDDP for Approximately 50 ms	33
Figure 37:	TIVA (Thermally Induced Voltage Alternation) Measurement of the Chip Reveals	
	Circuitry which is Sensitive to the Substrate Current	
	Topology of the Circuit which is Sensitive to the Negative Current Injection	34
Figure 39:	CDE Waveform for 10 m, 20 m, and 40 m Long Cables after they are Charged	^ -
E: 40	with Voltages Corresponding to the CDE / TLU trigger Threshold of TC2_IO1	35
Figure 40:	TLU Threshold Trigger Current (Negative Polarity) of IO1 Pin of TC2 versus	
E: 44	Duration of the Trigger Pulse (81104A, tr = 10 ns) at 100 °C Ambient Temperature.	
	Bond Wire Damages on an Automotive Power Device due to TLU	
	Emission Microscope Spot Showing the Trigger Mechanism	38
Figure 43:	Diagram of an IC in an Automotive Application Which Latched up during an	~~
	EOS Test on Supply Pin UBAT	39
Figure 44:	Due to the EOS Overvoltage at the Supply, the Parasitic NPN was Triggered that	00
Fig 45	Caused a Permanent Current Is to Flow on the Supply	
Figure 45:	Parasitic Structure in the Chip	40
rigure 46:	Cross Section of the Parasitic npn Which was Triggered in Result of the EOS	40
	Test in a Car	40

Figure 47:	PFA Picture of the High Voltage Power Clamp of XDSL IC Product and	
	Schematics	
Figure 48:	Electrical Characterization of the HV SCR Power Clamp	42
	Transient Latch-up Analysis of XDSL IC at Supply Line	
	Couple of Cells within the Digital Part Latch; Zoomed Section of TLU	
	•	44
_	EOS on Returned Part Inside VSS Pad; EOS Hard Latch-up at Metal and LDO	45
	Soft Latch-up Condition (LDO); Soft Latch-up Condition (LV Part)	
	Scope View Showing the Voltage Ringing on VDD_HV after the Latch-up Load	
_	on the LV-I/O Causing the Instability of the LDO	46
Figure 55:	Trigger Current during Positive Event; Circuit in Latch Condition	46
	EOS Fail Inside RC Clamp; Simulated TLU	
	Analog I/O P-Channel MOSFET EMMI Photon Emissions	
	Analog I/O Latch-up between PFET Pull-up and Adjacent Decoupling Capacitors	
Figure 59:	Power Management Product Output Driver Weakness due to Transient Latch-up	50
	Shoot through Caused by Glitch on SW1 Causing Bounce on PGND and PVIN	
	DC-DC Converter Failure of the NMOS Output Driver Circuit	
	Audio Output Driver Application	
	PC Audio Short Circuit Test Setup	
	Measurement Detail of Activating Short Circuit Protection with Current below	-
	Level Which Would Result in MN1 Damage (ORNF Ringing but Staying Stable)	53
Figure 65:	Measurement Detail of Activating Short Circuit Protection Resulting in MN1	- •
94.0 00.	Damage (ORNF Failing)	54
	Damago (Ortar raming)	О -Т