ESDA ONLINE ACADEMY FULL COURSE CATALOG COURSE ABSTRACTS

3D Integration with Through-Silicon Via (TSV) (1 Hour)

3D integration with through-silicon via (TSV) is a promising candidate to perform integration options with chip and/or wafer level stacking are emerging as the next generation of technologies that will continue to drive performance, power reduction and form factor shrinkage [1][2]. Some key advantages of the 3D integrated circuits are reduction of interconnect length which leads to improved interconnect delay, higher bandwidth/lower power, rapid access to memory, wide range of heterogeneous integration possibility, smaller Form-Factor etc. TSV fabrication is the key technology to permit communications between various strata of the 3D integration system. Hence understanding of TSV fabrication steps, such as etching, isolation, metallization processes, and related failure modes is important for 3D ICs. Per ITRS Roadmap [3], ESD protection of the core logic devices is identified as a critical challenge for the 3D process sequence. Hence proper understanding of ESD protection levels is also required for 3D integrated chip-to-chip signals with the goal of minimizing impact (area and latency) of 3D chip-to-chip connections. All such aspects and multiple other work related to 3D integration and ESD will be discussed and reviewed in this tutorial.

Advanced ESD/EMI Auditing Techniques (1 Hour) FC363

In order to solve today's ESD problems, ESD auditing must provide data on not only the static charge and voltage on tooling and devices, but also the transient voltage, current and electromagnetic field interference (EMI) up to at least 1 GHz. This practical course will teach how to use a variety of charge, current, voltage and E-field probes to understand the ESD/EMI threats during processing of ESD sensitive devices.

Advanced HBM – Dealing with Tester Parasitics, High Pin Count and Two Pin Testing (1 Hour) DT300

Certification: DT

This tutorial provides an overview of the joint HBM standard by the ESDA and JEDEC which introduces numerous options to set up the test plan for HBM qualification. The options include high pin count devices, reducing relay capacitance from the tester and two pin testing. There was a need to explain these options in detail and a user guide has also been released to provide further guidance in these tests. This tutorial will attempt to cover the user guide and will give examples of setting up the different tests plans that utilize the options outlined in the standard.

Basics of ESD Process Assessment (3hours) FC391

This tutorial gives an introduction to the approach and measurement methodologies for ESD process assessment and ESD risk analysis in typical production processes in semiconductor, printed-circuit board (PCB), and electronic system manufacturing industries. To large extents, the tutorial follows the ESD process assessment approaches described in ANSI/ESD Standard Practice SP17.1.

The tutorial summarizes the relevant physical parameters, for example, resistance, charge, electric fields, capacitances, resistances, discharge currents, and ESD event detection by EMI. The influence of these parameters on the ESD risks caused by charged personnel, charged devices and boards, and ungrounded conductors is discussed. Also, measurement techniques are explained in detail together with their limitations for the different process steps and strategies for an efficient ESD risk assessment. The application of those measurement techniques to assess possible ESD risks and to solve ESD problems are explained using theoretical and real-world case studies from many of the processes mentioned above. Examples of possible mitigation strategies are discussed with the attendees. The tutorial includes practical demonstrations and a hands-on session for the attendees to get experience and learn pitfalls of the most important measurement techniques used in ESD process assessment.

CDM Testing Essentials (1 Hour) DT200

Certification: DT, EDEC

This tutorial will give students the fundamental information required to quickly learn the CDM testing method on commercial CDM test equipment and the associated oscilloscope / metrology chain information needed to capture and interpret CDM waveforms. Additional information on CDM testing standards and their hardware differences, package effects on the CDM waveforms and package limitations will be covered. Students will also be introduced to the background information needed in understanding CDM failure modes along with test program output failure types needed to understand the effects of CDM testing.

Charged Board Events: A Growing Industry Concern (1 Hour) GP230

A charged board stores much more energy than a device (IC) because its capacitance is many times larger. In fact, the charge (energy) transferred in the event is so large that it can cause EOS-like failures to the components on the board. In this seminar, this board-level ESD event will be compared with the component level CDM ESD event. The waveforms from both ESD events will be compared and it will be shown that for the same voltage, the current in the board-level ESD event will be much higher than that from the chip-level ESD event. A summary of literature and industry data will be given. It is suggested that failure analysts give stronger consideration to these types of board level events before assigning an EOS diagnosis to the failure. This will support more effective root cause analysis and prevention of these failures.

Charged Device Model Phenomena, Design and Modeling (3 Hours) DD200

Certification: DD

This course teaches basic ESD circuit design concepts and ideas required to design ESD protection for Charge Device Model ESD tests. The course covers a brief history of CDM ESD development, charge and discharge physics, characterization methods, CDM failures mechanisms, and CDM design-in strategies.

CDM ESD circuit design approaches and simulation setups for CDM failure debugging are presented in this tutorial on the basis of case studies. Insight into CDM circuit simulation requirements and physical aspects of the CDM ESD phenomenon that are important for reproducing the event with circuit simulation will be taught and modeling approaches for CDM specific device physical effects necessary for accurate circuit simulation will be introduced. This course also teaches methods for simplified CDM circuit simulations where detailed information is either not available or too complex to simulate.

The course focuses on what type of circuits fail during a CDM discharge event and teaches the different types of ESD design circuit strategies that can be applied to protect those circuits. This class covers basic to advanced topics for CDM ESD design, but the student is assumed to already have a basic understanding of the CDM test method.

Learning Outcome

The attendees of this class are expected to have an improved understanding of the basics of charging of an IC component, CDM discharge event physical effects, internal circuit damages caused by the voltage and current during fast transient discharges and basic high current properties of ESD protection circuits in the CDM time domain. They should have an improved appreciation of circuit simulation methods for designing CDM ESD protection and for debugging failures caused by CDM ESD with circuit simulations. They should be able to apply ESD design strategies as discussed in the tutorial that have proven to protect ultra thin gate oxides of input circuitry and of devices connecting to signals that cross power domains techniques and strategies to protect cross domain circuits.

Circuit Design - Pcell, Clamps Design, Different ESD Protection Concept (3 Hours) IF21-4

This tutorial provides ESD circuit design principles for students with sufficient background in circuit design to apply these principles to specific applications in foundry process technology. The basic principles of the necessary design requirements for the ESD protection circuits and padring architecture will be discussed. The ESD engineer must understand the powered-on, reliability, and functional requirements for these circuit blocks. ESD circuitry has additional layout and design verification requirements. There are essential design for manufacturability (DFM) rules that apply to ESD-safe practices. These are discussed and expanded into ESD design best practices that circuit design engineers must follow. The ESD protection of advanced technologies is discussed, including the protection of FinFET technologies and RF circuit protection.

Circuit-Level Modeling and Simulation of On-Chip Protection (3 Hours) DD300

Certification: DD

This tutorial addresses modeling of on-chip ESD protection devices and simulation of ESD protection networks. The primary focus is SPICE-type simulation with compact (physics-based) models but a brief survey of other modeling approaches and simulation techniques will be provided.

The physical operating principles of commonly-used ESD protection devices will be examined. The high-current characteristics and transient responses of those devices will be explored to ascertain what behaviors should be captured by a model intended for circuit-level simulation of ESD.

Specific examples of model implementations will be provided. Techniques for circuit-level modeling of self-heating will be presented. Parameter extraction and model scalability will be addressed. This tutorial assumes some familiarity with device physics. It is directed toward persons with interests in semiconductor device physics, electronic design automation, and on-chip ESD protection circuit design.

Learning Outcome

After completion of this tutorial, a student should know how to set up a netlist for simulation of an on-chip ESD protection networks. Students will have the necessary background to start developing their own compact models and will be familiar with resources for Verilog-A model development.

Cleanroom Considerations for the Program Manager (3 Hours) FC110

Certification: PrM

Cleanrooms and clean environments are enabling technologies required for the manufacturing of many products that have exacting contamination control requirements in order to achieve defined yield and reliability targets. Clean manufacturing is required in the semiconductor, hard disk drive, flat panel display, and pharmaceutical industries, to name a few. Requirements of cleanroom and clean environments, and tooling therein, result in low humidity levels, low surface contamination levels, use of process-required insulators, and a lack of natural ions in the controlled environment. These factors can contribute to the development of elevated static charge levels in close proximity to sensitive products, presenting both a contamination and electrostatic discharge exposure.

This tutorial will provide a detailed review of the following concepts:

- Cleanroom and clean environment function
- Airborne particle classification standards
- Cleanroom compliance monitoring test methodologies
- Electrostatic attraction relation to airborne and surfacecontamination
- Electrostatic discharge concerns
- Cleanroom static charge generation challenges and control methodologies
- In addition, several case studies of static charge control issues in clean environments will be presented.

Compliance Verification: Pitfalls of Auditing (1 Hour) FC211

Accurate data is the foundation of effective ESD Program Management. Therefore, it's important to have confidence in the measurements. Choosing the correct type of equipment for each measurement is also important and not always obvious.

The class will cover the correct use of static locators, resistance meters, event detectors, and how to use ionizers effectively. We will discuss the various pitfalls of commonly used instruments, and the invalid test results that can result. For instance, static locators can yield totally invalid readings when used incorrectly due to voltage suppression. What you learn will help you avoid frequently encountered auditing problems, and improve your compliance verification program.

Controlling ESD in Automated Equipment by Proper Grounding (1 Hour) FC180

This course will focus on the grounding and material requirements of ESD Controls in Automated Handling Equipment (AHE) for prevention of CDM and MM type damage to ESD sensitive devices. Design methods and material selections that provide effective ground paths through the assembly will be introduced. Test methods used to qualify the design will be discussed. Students will also become familiar with different types of plating and practices to provide effective designs.

Design Constraints of ESD Circuits for High-Speed Applications (1 Hour) IF21-2

This tutorial discusses how CDM affects high-speed design. This presentation covers various circuit challenges in designing ESD devices as well as choices in protection. Future issues and different approaches to these challenges are explored. Additional information on how successive technology advancement impacts ESD design and a new methodology for CDM qualification of interface IP is presented.

Developing a Compliance Verification Program (1 Hour) FC241

Compliance verification is one of the required elements in the ANSI/ESD S20.20 standard. Without periodic verification of the ESD materials used within an Electrostatic Protected Area (EPA) programs can degrade over time. This course will cover some of the items that need to be considered for a successful compliance verification program.

Topics covered in this program include,

- What is a compliance verification program?
- What is the difference between product qualification and compliance verification?
- How does the ESD program manager determine the frequency of testing?

As part of the course, common ESD control items will be covered and how to do the testing efficiently and to meet the requirements of ANSI/ESD S20.20 and TR53. Questions can be submitted in advance to be answered as part of the course.

Device Stress Testing Standards Update (1 Hour) DT202

Certification: DT

This tutorial will describe major updates to the HBM and CDM Device Stress Testing Standards. After a brief introduction to both the Joint ESDA/JEDEC HBM and proposed Joint CDM Standards and the motivations for their developments, specific improvements in each standard (relative to their previous separate ESDA and JEDEC standards) will be described. These stress testing method improvements will be supported by test setup and measurement data where appropriate. Examples of the HBM and CDM stress testing procedures (setting up, measurement) using the new updated standards will be given. After taking this course, students will have the basic understanding of the improvements in the Joint HBM and proposed Joint CDM Standards and a basic understanding of how to apply these improvements to existing testers for stress testing.

Device Technology & Failure Analysis for the Program Manager (3 Hour) FC220

Certification: PrM

This tutorial provides an overview of the device design and fabrication technology of integrated circuits and other potentially ESD-sensitive devices; the basic concepts and techniques used to provide built-in ESD protection; and Failure Analysis (FA) techniques to determine the root causes of failures of device due to ESD. This class does not go into the depth necessary to equip the student to be an ESD Protection Designer or an ESD Failure Analysis Engineer. It does familiarize the student with the terms and concepts of ESD protection and FA to allow the student to interact with and understand the work being done by the Designer or Failure Analyst. After completing this tutorial, the student should be able to understand the basics of device ESD protection design and some of the trade-offs inherent in that process. The student will also become familiar with the commonly used failure analysis techniques and tools used to identify the root cause of an ESD failure. The common ESD Models (HBM, CDM), characteristics of ideal and real-world ESD protection are described. In addition, the broader topic of failure of devices due to more general electrical stresses is introduced. The terms electrical overstress (EOS) and electrically induced physical damage (EIPD) are defined with aim of understanding how ESD failures can be distinguished from other stresses.

Device Testing Correlation to Root Cause Failure Analysis (1 Hour) DT230

ESD Device Stress Testing is known to benefit at least three areas: qualifying the product, simulate failures from factory or field, and to improve the design of the product. Three ESD models (HBM, MM and CDM) are used to simulate failures and to differentiate between the different types of ESD failures and also to differentiate the ESD type failures from EOS-type failures. Even though there are no Failure Analysis standards for ESD, there is enough archived data, published data and experience to show correlation exists between the ESD Stress testing types, the physical failure types and the eventual root cause. The type of equipment required to get to the physical failures and see the failures will be emphasized. The class will show how to correlate each ESD model stress testing results to the physical failure type and the physical failure location on the die. A real example will be used to show how the ESD stress testing lead to the root cause of a field failure.

Electric Fields and Particles: Practical Considerations (1 Hour) FC262

ANSI/ESD S20.20 requires that process essential insulators with a measured electrical field strength of >2000 volts at 1 inch be kept a minimum of 12 inches from ESD susceptible items. Just what are the practical considerations of this statement? What about electrical fields of 1999 volts at 1 inch? Can items with lower field strength be ignored? Is there a size consideration when it comes to charged objects? If so, what is the size of a charged object that imposes a risk? What is the magnitude of an electrical field that should be of concern in a process?

This tutorial presents information from a recent investigation of electrical field strength that was conducted to support a revision of ANSI/ESD S20.20. The audience should gain a practical perspective of size and distance as related to electrical field strength. Additionally, the audience should be able to relate the information in this tutorial to their own process environments to help estimate the risk of damage to sensitive items that may be grounded within the electrical field from process essential insulators.

Electrical Overstress (EOS) in Manufacturing and Test (3 Hour) FC360

Electrical overstress (EOS) is a major cause of device failure in manufacturing and in the field. Despite this, there is relatively little information on the sources of EOS and on prevention practices, particularly for the factory. In this tutorial, the fundamentals of device overstress are reviewed. Relationships among device EOS stressing models, such as the Wunsch-Bell curve, are discussed. The causes of EOS and EOS-like events in manufacturing are described and categorized by source and by stress-type. The difficulties in distinguishing between power-induced EOS and high current ESD events such as charged-board events (CBE) and cable discharge events (CDE) are discussed. Case histories, including failure analysis and root cause determination, are presented and the few relevant industry specifications are reviewed.

Electrostatic Attraction (1 Hour) FC260

This training will cover the causes and effects of electrostatic attraction (ESA) and the solution to ESA problems in a variety of industries. Electrostatic attraction problems plague industries from photographic to medical and electronics. In the electronics industry alone, electrostatic attraction problems can be found in disk drive assembly, wafer fabrication and PC board assembly. The solutions to these problems can be found by applying a combination of the fundamentals of electrostatics and contamination control. An overview of clean rooms, ionization, materials and the control of static electricity will be presented. Real world problems and their solutions will be discussed using case histories.

- Basics of electrostatics
- Types of bonding
- Physics of electrostatic attraction
- Industrial problems
- Solving electrostatic attraction problems
- Case studies

Electrostatic Calculations for the Program Manager (4 Hours) FC380

Certification: PrM

This tutorial focuses on the basic mathematical formulae, calculations of use to the program manager. The content is at the introductory college pre-calculus and introductory college physics level with emphasis on electrostatics and basic electronics concepts. It is suggested that the student gain some familiarity with these subjects prior to the tutorial. Topics covered include the electrical charge, the electric field and Coulombs law, electric potential, and voltage, decay equations, and definitions and calculation of resistance and capacitance. Basic equations and relationships are explained to enable the application of the fundamental relationships. The fundamental equation, Q = CV, is used to explain charge sharing in real world situations. RC decay is discussed as it relates to ESD discharge from humans, devices, wrist straps, and materials and to air ionization. Simple models are used to compare models for various types of ESD (Human-Body Model, Charged Device Model and others) and provide a conceptual understanding of the differences among the calculations for peak current, power, energy, and threshold voltage for a simple device.

Electrostatic Discharge Effects in Integrated Circuit Technologies (1 Hour) DD104

This course will outline the fundamentals of ESD phenomena and the methods to control the effects of ESD for safe manufacturing of IC devices. The training material will include the nature of ESD transients, their impact on the IC devices, common methods to test for ESD at both the device level and the system board level, and the overall protection techniques. Finally, the course will review the advances in IC technologies that lead to future challenges for ESD development and the resulting important technology roadmap established by the ESD Association.

EOS - A Big Challenge in Today‘s Handling of Customer Rejects (1 Hour) GP250

Handling of customer rejects has become more and more challenging over the years in view of EOS. Unlike ten years ago today most customers are asking for an EOS statement containing a conclusive and comprehensive explanation of the failure scenario that has finally resulted in an “EOS-like” damage and this EOS statement has to be discussed on much higher technical level. On the other hand still today there is not much awareness on the customer side that most “EOS-like” failure signatures do not allow a comprehensive conclusion to the origin of EOS and so the final root cause cannot be evaluated without customer’s support. But in order to be prepared to conduct a successful root cause analysis together with customer the supplier is committed to build up an EOS knowledge base for both internal and external needs. The seminar should deliver insight in today‘s handling of customer rejects in terms of EOS and all the background that is necessary to be successful in that important topic – complemented with a few demonstrative examples.

EOS: A New Focus (1 Hour 30 minutes)

Electrical Overstress (EOS) accounts for most of the electrical failures of devices that occur in factories and in the field. One EOS root cause, ESD, has received much attention in technical literature, standards bodies and educational workshops and tutorials. It has been approached in a systematic manner which has resulted in relatively successful practices for design of robust devices and control procedures for the factory. However, the same cannot be said for the effects of the broader categories of electrical stresses that can be the root cause of electrical overstress. These other root causes (over-voltage, over-current, over-power), when grouped together, are more prevalent causes of failure than ESD by a wide margin because of the lack of a coherent design and mitigation strategy. One of the main reasons for this is that EOS root causes are widely varied and very application dependent. As a result, no simple broad models for EOS have emerged comparable to HBM and CDM for ESD. Common device design practices have not been developed to the same extent, system level approaches tend to be ad hoc and responsibility for controlling potential sources in manufacturing tends to be diffused or non-existent. In this webinar, we review the current status of work on EOS. This will include recent significant reports in the technical literature, work of standards and industry groups and some recent interesting case histories. We will also explore the definitions of EOS and some related terms and attempt to clarify some common ways these terms are misused in literature and in failure analysis reports. “Rethinking” how we talk about EOS will help Failure Analysis, Design and Manufacturing work together to reduce EOS-induced failures (including ESD).

ESD Basics for the Program Manager (5 hours) FC100

Certification: PrM

This tutorial provides the foundation material for understanding electrostatics and ESD and their role in the manufacturing and handling of ESD sensitive devices. The fundamental properties of charge, electric fields, voltage, capacitance, and current are discussed with a view towards understanding key electrostatic phenomena and electrical processes. These include charge gener ation and decay, material properties, and induction. An overview of device failure mechanisms is presented, including how these models impact ESD control programs. Finally, the course provides an overview of ESD control procedures during handling and manufacturing and an overview of ANSI/ESD S20.20 program requirements. This full day course is required for those in-plant auditors and program managers who are working toward professional ESD certification. The presentation includes many in-class demonstrations, videos, and animated slides.

Some sample topics covered in this course are:

- Definitions and relationships among important electrical and mechanical properties
- Causes of charge generation and decay
- Field effects and voltages
- Role of capacitance in ESD (Q=CV)
- Overview of key measurements including common pitfalls of some measurements
- Review of ESD failure models
- Understanding and demonstrating electrostatic induction
- Utility and limitations of air ionization
- Basic goals of ESD controls
- Properties of effective ESD control products and materials
- Overview of ANSI/ESD S20.20 ESD program development requirements

Learning Outcome

- An understanding of several concepts that are included in the ESD Program Manager Certification Exam
- A deep understanding of ESD fundamentals that are vitally important for developing and managing sound ESD programs
- Students will learn effective techniques for demonstrating a wide range of ESD fundamentals
- Students will learn how to evaluate materials for CDM mitigation properties and much more

ESD Circuits (3 Hours) DD100

This tutorial will focus on several clamp approaches including BigFETs or RC clamps, snap-back NFETs, diodes, SCRs including HV SCRs, low capacitance clamps methods, including those for MOSFET based LNAs and cross-domain clamping. Spice simulations and simple models, where applicable, will be used to design and analyze circuit performance. Models include HBM, CDM, and IEC sources, gate pull requirements for dynamically lowering snap-back thresholds, and diodes. Gate pull for snap-back NFETs will include cascade and stacked NFETs. The need for NQS MOSFET models will be discussed with respect to CDM simulations. Operational characteristics of diodes will be examined, including simple models and turn-on delay. Diode types to be examined include STI, gated, and gated with LDD block. Protecting RF transceiver switches will be studied and will include spice simulations and the design of low capacitance snap-back NFETs. The cross-domain analysis will feature SPICE-based gate oxide rupture models.

Learning Outcome

The attendee will learn how to design BigFETs clamps, gate pull snap-back clamps, types of SCRs, and circuit protection networks. There will be an emphasis on circuit simulation for design and circuit models including failure mechanisms, tester models, pin interconnect parasitics, and diodes.

ESD Device Qualification Testing (3 Hours) DD240

Certification: DD

This tutorial addresses the details of both Human Body Model (HBM) and Charged Device Model (CDM) qualification testing. This course will help in interpretation of the HBM joint standard JEDEC/ANSI/ESD JS-001-2014 including the following details: Waveform verification, understanding of Table 2A (minimum required set of pin combinations) and Table 2B (legacy pin combinations), pin categorization and pin grouping, I/O pin sampling, stress plans details including efficient testing (reduction in pin count) and some debugging options. In addition, this course will discuss CDM testing details regarding waveform verification, stress plans, peak current (Ipeak) variability and how does it affect the testing results, and debugging options as well as an overview on the new CDM joint standard JEDEC/ANSI/ESD JS-002-2014.

Learning Outcome

The attendee should come away with a stronger understanding of both human body model (ANSI/ESDA/JEDEC JS-001 - HBM) and charged device model (ANSI/ESDA/JEDEC JS-002 – CDM) testing specifications and the requirements called out in each of these specifications. For HBM this includes a better understanding of Table 2A and Table 2B and the use of association in Table 2A as well as opportunities to minimize test time and an understanding of cloned IO requirements. For CDM this includes a better understanding of the waveform verification requirements and the impacts of an air discharge on product qualification.

ESD from Basics to Advanced Protection Design (1 Hour) DD110

Certification: DD, EDEC

This course gives a comprehensive overview from ESD basics to ESD on-chip design principles, covering up to the latest silicon technologies appealing to a variety of engineers from design to process technology and failure analysis to quality. The attendee will have an in-depth understanding of the principles of ESD device design along with a full perception of what it takes to address almost every kind of design scenario, how to apply rules of thumb for successful on-chip design, knowledge of lessons learned from case studies, and empowerment to communicate with customers on ESD quality issues. In its complete ESD overview, the course emphasizes on-chip protection methods, including an understanding of any interactions to the eventual system protection.

Learning Outcome

This course uniquely provides a complete picture of the ESD phenomena from A to Z, from component to system ESD issues. It is specifically aimed at beginning ESD designers to become familiar with the basics of ESD design parameters and ESD physics. It should be also attractive to those who already have some knowledge but wish to expand it by learning about some of the advanced designs and various protection schemes for different applications such as low voltage CMOS and high voltage analog. After taking this class the ESD designer should be able to choose the proper protection option and estimate its performance to meet the target ESD levels.

ESD Fundamentals I for Stress Testing (1 Hour) DT140

Certification: DT

This tutorial is part 1 of a condensed version of the ESD Basics for the Program Manager tailored for technicians and engineers who direct or perform ESD stress testing at the device and system level. This tutorial provides the foundational material for understanding electrostatics and ESD along with their role in the manufacturing and handling of ESD sensitive devices. The fundamental properties of charge, electric fields, voltage, capacitance, and current are discussed with a view towards understanding key electrostatic phenomena and electrical processes; these include charge generation and decay, material properties, and induction. An overview of device failure mechanisms is presented, including how these models impact ESD control programs.

ESD Fundamentals II for Stress Testing (1 Hour) DT141

Certification: DT

This tutorial is part 2 of a condensed version of the ESD Basics for the Program Manager tailored for technicians and engineers who direct or perform ESD stress testing at the device and system level. This tutorial provides the foundational material for understanding electrostatics and ESD along with their role in the manufacturing and handling of ESD sensitive devices. The fundamental properties of charge, electric fields, voltage, capacitance, and current are discussed with a view towards understanding key electrostatic phenomena and electrical processes; these include charge generation and decay, material properties, and induction. An overview of device failure mechanisms is presented, including how these models impact ESD control programs.

ESD Parameters for the Foundry, IC Designer and IP/EDA Vendor (3 Hours) DD208

ESD devices and protection circuits should demonstrate an effective shunting and clamping of ESD stress in ICs and electronic systems. It should also not influence the proper functionality of the protected system. The trade-off between ESD capability and signal integrity is reflected in key ESD parameters extracted from dedicated measurements. The ESD protection, planned at IC design level, requires information and data exchange between foundry supplier, IP vendor, and IC designers, and EDA tools vendors. This tutorial aims in guiding the ESD engineer in the foundry in the process of creation and supplying the ESD portion of the PDK. In particular providing a variety of special parameters required for design of an optimized ESD protection. This includes an overview of benchmark key ESD parameters, test structures, measurements, extraction methods, and useful presentation of the information. The designer and the EDA tool vendor are equipped with the know-how of using the parameters in optimizing the ESD window as well as developing effective methods of proper ESD protection, ESD checkers and simulations. As part of this tutorial, two technical reports ESD TR22.0-01-14 (Relevant ESD foundry parameters for seamless ESD design and verification flow) and ESD TR22.0-02-18 (ESD parameters from Intellectual Property (IP) providers), written by ESDA 'ESD parameters' WG-22, are reviewed.

Learning Outcome

- Learn about the required ESD-related deliverables that the foundry should provide to its design customers and IP/EDA tools vendors. In formal words, the ESD ingredients of the Process Design Kit (PDK).
- Understand the benchmark methods for creation and extraction of ESD-related data, including test-ctructures, measurements procedures and tools, as well as presentation of key parameters, curves, etc. This know-how covers a variety of technologies ranging from CMOS, RF, embedded NVM to high voltage BCD.
- Learn about possible monitoring of ESD parameters, protection performance, interference to normal operation, and robustness to process variation.
- Exposure to the inter-relations between the foundry, the IC designer, and the IP and EDA tools vendors, from the ESD perspective. In particular, the data exchange between foundry supplier, IP vendor, EDA tool vendor, and IC design integration.

ESD Problem Solving (1 Hour) GP331

It's Friday at 3:00 and your quality manager calls you, "We are having ESD failures." Now what do you do? Go out and audit your line? This online course will outline the steps that you should take to examine your process before you audit your line or even leave your office. A systematic approach will be explained on the logical steps to take for ESD troubleshooting. Only after such an analysis should you go on the line for measurements or assessments.

ESD Program Development and Assessment (ANSI/ESD S20.20 Seminar) FC340

Certification: PrM

This seminar provides instruction on designing and implementing an ESD control program based on the newest release of ANSI/ESD S20.20. The course provides participants with the tools and techniques to prepare for an ESD facility audit. This two-day course is an ESDA certification requirement for in-plant auditors and program managers who are working toward professional ESD certification.

The following topics are covered in this course:

- Overview of ANSI/ESD S20.20
- How to approach an assessment
- Administrative elements
- ESD program assessment
- ESD program techniques for different applications
- Technical elements
- Overview of the assessment process
- The audit checklist and follow-up questions

ESD Protection and I/O Design (3 Hour) DD201

This tutorial is intended to provide the attendees with the tools to take a device and circuit level understanding of ESD protection methods and implement them effectively in I/O designs for CMOS bulk technologies. Beginning with a review of common ESD protection strategies, this course will focus more directly on how to build ESD-robust I/O cells and how to integrate them on a full chip. The tutorial will cover various types of I/O pads including analog, RF and digital pads. Different types of ESD protection strategies and their usage in I/O pad cells will be described, for example rail clamp, self-contained, and SCR based protection schemes. This course will also discuss the decisions and challenges which ESD and I/O designers typically face when designing I/O pads. More complex ESD solutions will also be described such as stacked rail clamps, ghost rails, and protecting signals that can swing below ground or above the supply. Finally, this tutorial will touch on various supply schemes including multiple power domains and isolated grounding schemes. It will end with discussing pad ring construction aspects for both wire-bond and flip-chip packages.

ESD QMS Best Practices Strategy Including Class 0 and Costly Controversial ESD Myths (3 Hours) FC166

Part I: ESD QMS Best Practices Strategy Including Class 0

While most companies are acutely aware of the hazards of ESD (electrostatic discharge), few are aware that the ESD QMS Strategy is equally important as the technical requirements. This is especially true for the extreme ESD sensitivities of Class 0 since the trend toward Class 0 devices is escalating rapidly. Furthermore, most companies do not know what their device sensitivities are because 90% of IC datasheets do not include CDM Sensitivity data. The absence of this data and the lack of understanding of ESD QMS best practices has reached a critical stage.

S20.20 (ANSI/ESD S20.20) is the best industry standard available and is an excellent foundation for ESD QMS best practices programs. However, companies with advanced technologies have found they must customize the technical requirements of S20.20 and introduce sound ESD QMS practices to avoid unacceptable failure rates in the factory and field. Join us for this interactive presentation and learn if you are at risk and how to establish a robust ESD QMS strategy. You will also learn how to obtain ESD CDM & HBM device sensitivity data as well as how to prepare for Class 0.

Part II: Costly Controversial ESD Myths

There are several common misunderstandings and controversies that can have significant impact on costs, quality and reliability of ESD programs. These misunderstandings or "myths" often result in costly unnecessary expenditures and/or a compromise of the program integrity. These same myths are cited by skeptics who do not fully understand the physics involved. Consequently, it is important to identify and dispel these myths.

Latency is a significant reliability consideration that is surrounded with controversy. Some experts will argue that latency is virtually non-existent while others claim that it is the dominant failure mode. Join us for this highly interactive discussion and learn about Latency as well as common myths such as:

- Myth: Circuit Boards are Less Sensitive to ESD than Devices
- Myth: HBM Data Are Sufficient for Determining Device Sensitivity Levels
- Myth: MM Is A Valid Simulation Related To Machines
- Myth: Air Flow Causes Charging
- Myth: Metalized or Highly Conductive Shielding Layers Are Essential
- Myth: Humidity Control is Essential for ESD
- Myth: Latency Failures Comprise 90% of ESD Failures

Learning Outcome

- A Deep Appreciation for The Importance of A Solid ESD QMS Strategy
- How To Include Class 0 In The QMS Strategy
- The Importance of Fully Understanding ESD Fundamentals and Advanced Technology
- How Many ESD Myths Can Disrupt the Best of ESD Programs And How To Prevent This From Happening
- A Review of Important Technical Concepts Such as CDM And CBE

ESD Solutions for RF Applications (3 Hours) IEDS21-1

While designing circuits for complex applications can be challenging, RF circuits present additional requirements on the designer. Not only are these circuits very sensitive to ESD threats, but adding ESD protection will invariably compromise performance. Thus, in most cases, the design of functionality and ESD protection must be done as co-design. This seminar will address the various aspects of advanced ESD design. This will then be extended to RF applications and ESD co-design. Finally, this seminar will discuss various case studies to illustrate the principles presented.

ESD Standards Overview for the Program Manager (3 Hours) FC210

Certification: PrM

Standards provide the foundation for building an ESD Control Program. Many of the individual tutorials within the Program Manager Certification curriculum discuss specific Standards, Standard Test Methods and other standards related documents in depth. This Standards Tutorial provides an overview of all the ESD Association and other relevant industry and military Standards, grouped into common test types based on measurement probe and test instruments. A common methodology is used in this tutorial to cover the requirements, applications and specifications for each Standard and Standard Test Method. This course helps prepare students that will write the ESDA Program Manager exam.

Summary:

An overview of all the ESDA standards and related documents used in establishing an ESD control program and prepare the student for the ESDA Program Manager exam.

ESD System Level: Physics, Testing, Debugging of Soft and Hard Failures (3 Hours) DD231

The tutorial is an expanded version of the previous DD231 tutorial on system level ESD. The main difference is the addition of many experimental demonstrations, update of information, and in-depth discussion on problems of the IEC 61000-4-2 testing, with examples on how to perform this testing and obtain the best possible results and documentation. About half of the time will be spent on experimental demonstrations.

Topics will include:

- ESD physics: charging and discharging.
- System level ESD testing
- System level soft failure mechanisms and debugging
- Design for avoiding ESD problems

Learning Outcome

The seminar will enable the audience to better understand system level ESD testing such that meaningful, repeatable tests can be performed and data is gathered, that allows to identify the root cause of observed failures.

ESD Testing: Different TLP, Different IEC testing, Surge Test etc. (1 Hour) IF21-6

In this tutorial, testing of the human body model (HBM) and charged device model (CDM) is presented. Additional information on the basic concepts and measurement principles of transmission line pulse (TLP) are covered. This course also discusses system-level testing and problems with testing components outside the system

ESD Test Simplification with Approved Sampling Methods in HBM D-E (1 Hour) DT220

Certification: DT

Advances in semiconductor technology development have enabled significantly more complex integrated circuits (IC). This complexity has driven an increased number of pins on an IC package. These higher pin count IC packages have led to a significantly higher ESD qualification cost and complexity. However, many designs often have a large number of common or “cloned” IOs which enables the possibility of using statistical sampling schemes to help improve ESD qualification in an efficient manner without reducing the overall quality of the stress test method. This tutorial will discuss the details behind the changes that are being made to the joint ANSI/ESDA/JEDEC JS-001-2012 HBM Test Method, including the definition of cloned IOs, the procedure for sampled testing of cloned IOs and a clear statistical justification behind these changes. The tutorial will conclude with a discussion of possible future opportunities in both HBM and CDM test methods for even further improvements in using statistical sampling techniques.

Essentials for Controlling the ESD Work Area (1 Hour) DT143

Certification: DT

This tutorial focuses on the basic components of an ESD controlled work area and how to verify the correct operation of each component. Most ESD protected Areas (EPA) include grounded workstations (special mats or table tops) and personnel grounding techniques (wrist straps, constant monitors, heel grounders, footwear, conductive flooring and dissipative chairs). In addition, the proper use and testing of smocks and ionization will be covered.

Fundamentals of ESD System Level DD134 (1Hour)

Certification: EDEC

This tutorial is intended to help those tasked with designing and testing prod-ucts to system-level ESD standards by providing first an overview of what the real-world system ESD threats are and the associated standards that describe these events. Then detailed information on qualification testing is given on IEC 61000-4-2, the most widely used standard, but also ISO 10605 and other standards. This topic includes waveform verification, discharge points, test levels and result classification. System level characterization is broken into five different types including, testing of components outside a system, cable discharge events, charge board events, electro-magnetic field scanning and SEED – system efficient ESD design. The last part of the course dives into the design and simulation strategies for system level robustness where on-board and on-chip protection need to work together. The more popular components for on-board protection are presented and compared.

Learning Outcomes

After attending this tutorial one will understand the differences between the types of ESD events that occur during IC handling and assembly, board subassembly testing, and final system level operation. One will understand what the similarities and differences of on-board protection and on-chip protection are and how these need to work together to achieve system level robustness. Finally, one should be able to understand the overall design and characterization approaches to be able to create a robust system level solution for their products.

Fundamentals of Failure Analysis (1 Hour) DT142

Certification: DT, EDEC

Failure analysis is the diagnostic tool of the semiconductor industry. It is the semiconductor equivalent of forensic science. Failure analysis unravels the mystery behind how and why a part failed, determining the root cause and corrective actions needed to prevent future failures. This tutorial is targeted toward people doing stress testing on a daily basis where failures are generated and need to be analyzed to determine what failed and how to improve a part’s robustness. The focus will be on failure analysis methods and tools use to analyze failures resulting from ESD, TLP, or latchup related stressing but will be applicable for wearout as well as infant mortality related failures as well. The tutorial will cover the 5 basic steps necessary to perform a failure analysis: 1) Information Gathering, 2) Failure Verification, 3) Failure Site Localization, 4) Root Cause Investigation, and 5) Corrective Action.

Fundamentals of System Level Testing (1 Hour) DT130

Certification: DT

This tutorial provides an understanding of how testing done at the system level is essential to understanding the stress that will be applied to a device installed in the final product. This tutorial will cover the various system level testing standards including how the tests are performed and evaluated. Guidance is provided for applying these tests at the device level. Test results will be discussed and differences between hard and soft failures examined. In addition, a brief overview of tools available for root cause analysis at the system level will be examined.

Grounding in an Electrostatic Protected Area (1 Hour) FC231

Grounding is perhaps the single most important technical aspect in establishing an electrostatic protected area. The ESD Association grounding standard ANSI/ESD S6.1 provides potential users with specifications, guidance and suggestions for implementing a grounding/bonding system suitable for nearly any imaginable application. This information is not found anywhere else in industry literature. This web-based training session will include answers to the following questions:

- What grounding method is appropriate for a work area?
- What measurements are needed?
- Are there any new terms or definitions?
- What are the proper ways to ground personnel in the workplace?

Grounding in an Electrostatic Protected Area (1 Hour) Chinese (1 Hour) FC231

Grounding – Variations, Concepts, Nuisances, Equipment & Troubleshooting (3 Hours) FC121

Grounding for ESD control seems so simple, yet many times issues arise after a grounding strategy is implemented. This class will cover variations in grounding approaches, concepts to consider when employing a ground system, nuisances and how to troubleshoot them with the correct equipment.

Learning Outcome

- Understand the term “ground” and all of its associated meanings from the industry in order to test, measure and/or design effective ground systems.
- Understand the various ESDA standards and test methods in regards to measuring ground connections.
- Realize the reason for a Common Point Ground and how to achieve it.
- Determine the right amount of resistance, (not too little and not too much) for many ESD control situations.
- Determine how to troubleshoot typical ground issues in order to maximize productivity.

Human Body Model Testing Essentials (1 Hour) DT100

Certification: DT, EDEC

This tutorial addresses the details of Human Body Model (HBM) qualification testing. This course will help in interpretation
of the HBM joint standard JEDEC/ANSI/ESD JS-001 and will include the following details: Waveform verification, understanding of Table 2A (minimum required set of pin combinations) and Table 2B (legacy pin combinations), pin categorization and pin grouping and I/O pin sampling. Stress plan details will be discussed including efficient testing (reduction in pin count) and some debugging options.

High Speed Digital Oscilloscope Fundamentals (1 Hour) DT211

Certification: DT

This tutorial reviews the basic characteristics of oscilloscopes, general use of modern oscilloscopes and their specification as they relate to ESD measurements. Examples of measurements capturing waveforms and analysis on HBM, MM, HMM, CDM, and TLP waveforms will be presented. The basic specifications of a typical oscilloscope and their implications for accuracy on ESD measurements will be reviewed. Topics include sampling rate along with analog and digital bandwidth considerations.

Highlights and Key Concepts of Footwear/ Flooring Standards (1 Hour) FC181

Footwear/Flooring Systems can play a major role in a successful ESD Control Program. How do you properly select and implement an ESD Footwear/Flooring System? This course will provide an overview of the concepts and Standards used for product qualification of footwear and flooring, as well as compliance verification of a Footwear/ Flooring System. This course will focus on the Footwear/ Flooring Standards and Standard Test Methods related to selecting and implementing a Footwear/Flooring System for use an ANSI/ESD S20.20 Control Program.

Highlights and Key Concepts of Footwear/ Flooring Standards Korean (1 Hour) FC181

Highlights and Key Concepts of Footwear/ Flooring Standards THAI (1 Hour) FC181

HMM – System Level Testing of Components (1 Hour) DT131

This tutorial will explain in detail the intent of the HMM standard test method. The tutorial starts with the hurdles of testing components to the IEC 61000-4-2 standard. The scope and purpose of the HMM standard test method will be discussed. The waveform used in this test and its critical specifications are presented along with the qualified equipment used to deliver the waveform. Three test configurations are introduced to address equipment specifics and recommending grounding. The tutorial will also provide some data to show the measurement variability that this test method has.

How To's of In-Plant ESD Auditing and Evaluation Measurements FC101 (5 Hours)

Certification: PrM

Compliance verification is one of the most important elements of ESD program management and there are many technical and administrative pitfalls that can be avoided. The attendee will learn not only how to make valid auditing measurements in accordance with ESD TR53 – Compliance Verification of ESD Protective Equipment and Materials, but also how to rec ognize and avoid common pitfalls. Common instruments will be explained as well as the invalid test results that can result when they are used incorrectly. Advanced auditing techniques will also be covered that enable Class 0 devices to be handled successfully. There are many ways to administer effective compliance verification programs. Two successful examples will be presented that were developed independently by differ ent companies. Hidden administrative pitfalls that often result in poor compliance will also be discussed. This tutorial will be highly interactive with live demonstrations, in-plant photo graphs, and compelling video clips. Students will be encour aged to ask questions and to participate in the discussions.

Learning Outcome

- Understand auditing information included in ESD Program Manager Certification Exam
- Learn to make and correctly interpret auditing measurements based on ESD TR 53
- A deep understanding of five auditing options for sustaining program execution excellence
- Understand the critical requirements to successfully handle extremely sensitive Class 0 devices
- Develop real world solutions from the review of successful case studies and class discussions

Impact of Technology Scaling on Components High Current Phenomena and Implications for Robust ESD Design (3 Hours) DD311

Certification: DD

This advanced tutorial will focus on high-current behavior of stand-alone components, with the aim of optimizing effectiveness of ESD clamp devices (irrespectively of their schematic implementation) and maximizing the ESD SOA (Safe Operating Area). Components in both Analog and Digital technologies will be discussed, with emphasis on technology trends. This class is intended for individuals who have taken the basic on-chip protection class and are familiar with the basic device physics for both ESD and latch-up.

Learning Outcome

- Understand the physics of basic components under high current conditions with particular emphasis on scaling aspects (geometrical (i.e. W & L), power (following Wunsch-Bell power curve) and electrical (rise time)
- Understand how to experimentally extract high current characteristics
- To optimize ESD protection circuits based on fundamental components behavior

Integrated Circuit ESD Fundamentals (3 Hour) DD103

Certification: EDEC

This three hour tutorial is focused on integrated circuit ESD fundamentals, and is targeted for two audiences: the IC circuit designer who needs knowledge of how ESD can affect IC design, test, handling and system use; and those engineers wishing to be introduced to IC ESD, as a primer to further study.

The tutorial covers the following topics:

ESD Definitions

- Overview of the ESD Threat and ESD Controlled Workspaces
- ESD Stress Models and Standards
- Introduction to Transmission Line Pulse (TLP) ESD Testing
- ESD Design Window
- ESD Protection Network Design
- Power Clamp ESD Design and Tradeoffs
- Input Protection ESD Design
- Output Drivers ESD Design
- Switches (Transmission Gates) ESD Design
- RF ESD Protection
- IC ESD - Integration Issues
- CDM Protection Guidelines
- ESD Design Verification
- ESD Debug and Diagnosis

Learning Outcome

Upon completion of the tutorial, the student will have a basic understanding and impact of

- The ESD Threat to ICs and ESD Controlled Workspaces
- Device Level ESD Stress Models and Standards
- Transmission Line Pulse (TLP) ESD Testing
- ESD Design Window – proper region of operation for an ESD device
- Protection – Network Design, Power Clamps, Input / Output / Switch Protection
- RF ESD Protection Concepts
- ESD Element Whole Chip Integration Issues
- CDM ESD IC Protection Guidelines
- ESD Simulation and Design Verification Concepts
- ESD Failure Diagnosis and Failure Analysis Methods

Integrated ESD Device and Board Level Design (2 Hour) DD340

Efficient ESD design for system level ESD can only be achieved if board and device level protection circuitry coincide. The purpose of this tutorial is to develop an understanding of board/IC interaction under IEC 61000-4-2 testing conditions and to discuss useful design strategies supported by appropriate tools. This is meant to be beneficial both for ESD engineers of ICs and board designers responsible for EMC/ESD compliant design of the system. While it has clearly been pointed out that even elevated IC level HBM targets are insufficient for achieving the required IEC 61000-4-2 ESD level, more awareness has to be developed for the detailed turn-on and clamping behavior of IC level and board level ESD protection components. High current characterization of board protection and IO circuit by TLP is a first step. This enables the board designer to assess the behavior of IC pins and select appropriate board protection elements. The design optimization should be based on high current models of board components and IC IOs and the numerical simulation of the protection network under ESD conditions. Finally, various test methods are available to evaluate the efficiency of implemented protection on board level quantitatively

Learning Outcome

The attendee will understand the concept of SEED simulation and will be able to apply it to an own PCB /IC codesign simulation. This will allow the system design attendee to run a pre-hardware optimization of the board protection and it will enable the IC protection engineer to evaluate his protection concept regarding the available design window for system ESD.

Introduction to ESD Design in High Voltage Technologies (3 Hours) IEDS21-4

This seminar gives an introduction to ESD design in high voltage technologies for integrated circuits with pin voltages from 12 volts upwards. After a short introduction of typical applications and requirements, an overview of different technologies and the typical device portfolios in these technologies will be given. Different ESD protection concepts are introduced, analyzing advantages and disadvantages of the various possible approaches to implement ESD networks (diodes, snapback, active clamps…). Finally, HV-technology and design related challenges regarding ESD protection are discussed, with a special focus on relevant case studies.

Introduction to RF ESD Design (3 Hours) DD150

This tutorial is an introduction to RF concepts and RF ESD clamp design. It is intended for ESD engineers who do not have an RF background to learn the concepts needed to design effective protection circuits. The RF concepts include impedance matching and smith chart basics. RF amplifier operation and load line basics are presented to give a foundation for the RF ESD protection circuit design. The tutorial will also touch briefly on RF switches and filters. The second half of the tutorial will focus on designing an ESD clamp for an RF application. Concepts will be presented, such as calculating the turn-on voltage of the clamp such that it will protect the part but not turn on during normal, RF operation. A clamp's parasitics also need to be considered in an RF application so that the parasitics do not degrade the product's performance. Finally, some testing tools will be reviewed concerning testing RF products. The challenges will be highlighted, and different testing practices that are used in HBM, TLP, and IEC testing of RF products will be reviewed.

Learning Outcome

This tutorial is aimed toward those individuals who need to design ESD protection circuits for RF and millimeter wave applications. After completion of this tutorial, a participant will understand the fundamental RF concepts critical to designing RF ESD on-chip protection schemes. The participant will gain a basic understanding of how RF components such as amplifiers, switches, and LNA's performance metrics will impact the design of ESD clamps and why traditional digital and CMOS ESD clamps can degrade RF performance. Finally, individuals who take this tutorial will know how to design ESD clamps with components such as HBTs and PHEMTs for Gallium Arsenide (GaAs) and MOSFETs for Silicon-on-Insulator (SOI).

Ionization Issues and Answers for the Program Manager (3 Hour) FC120

Certification: PrM

The primary method of static charge control is direct connection to ground for conductors, static dissipative materials, and personnel. But a complete static control program must also deal with isolated conductors, insulating materials, and moving personnel that cannot be grounded. Air ionization can neutralize the charge on insulated and isolated objects. It does this by charging the molecules of the gases in the surrounding air. Whatever charge is present on objects in the work area, it will be neutralized by attracting opposite polarity charges from the air. This webinar will present the information needed to use ionizers to solve problems caused by static charge. It is a basic course on ionizers, providing an introduction to their use, as well as advanced application information.

Latch-up Fundamentals (1 Hour) DD112

Certification: DD

Latch-up continues to be of interest today in advanced CMOS, mixed signal (MS) CMOS, RF CMOS, BiCMOS and smart power technologies. Those attending this course will understand the fundamentals of CMOS latch-up. The course will focus on theory, test structures, application, experimental results, simulation and CAD design systems. Those attending will also understand the impact of design, semiconductor process and circuits on CMOS latch-up.

Latchup Physics and Prevention (3 Hours) DD214

Latchup has occurred in CMOS technologies since their inception and continues as a threat in modern finFET technologies. This course will begin with a basic overview of the latchup phenomenon and then dig deeper into the theory and physics associated with it. Latchup mitigation techniques will be reviewed along with the physics behind them. These will include both design and process techniques. The basics and pitfalls of latchup testing will be taught, along with an introduction into transient latchup. Proper wafer-level test structure design and characterization will be taught.

The primary audience for this course is design and reliability engineers tasked with designing for latchup success. Latchup test engineers will also benefit from a deeper understanding of latchup physics and design practices. The course assumes some familiarity with basic circuit design practices and semiconductor physics. Participants will leave with a deeper understanding of the physics behind latchup, its mitigation, and the impact of future technology trends on latchup susceptibility.

Learning Outcome

- Understand the physics behind latchup
- Understand how technology scaling impacts latchup
- Learn latchup mitigation strategies in design and process development and the physics behind them.
- Will learn best practices for test structure creation and measurement and how to translate the results into latchup design rules.
- Will understand the latchup test standard in the context of creating design rules to successfully pass the test as well as other real-world risks not covered by the standard.
- Learn latchup mitigation strategies in design and process development and the physics behind them.
- Will Learn best practices for test structure creation and measurement and how to translate the results M65into latchup design rules.
- Will Understand the latchup test standard in the context of creating design rules to successfully pass the test as well as other real-world risks not covered by the standard.

Latchup Testing and Troubleshooting (1 Hour) DT201

Certification: DT, EDEC

This tutorial focuses on latch-up testing and troubleshooting. Latch-up is primarily seen in CMOS and BiCMOS technologies but can be present in bipolar technologies. Resistance to latch-up is generally characterized during process development and design rules are implemented at device circuit block layout. Design checks for latch-up are often implemented but latch-up immunity is still mainly guaranteed by testing. This tutorial will help the student to understand the issues related to latch-up, ways to prevent it and methods used for verifying latch-up resistance in products.

Overview on Efficient and Reliable System-Level ESD (1 Hour) GP330

The ongoing integration of system functionality in ICs requires that IC pins comply with system-level ESD specifications. Often without knowing the final application, component-level ESD designers need to provide designs which are also robust to system-level ESD stress. In contrary, system-level ESD designer usually have no access to information about the component-level ESD protection design. To overcome this situation, the system-efficient ESD design (SEED) has been proposed. This online seminar introduces and evaluates two main system-level design methodologies: datasheet-based design and SEED (System-efficient ESD design). Different examples illustrate which data is used as design input and what are the limitations of each methodology. It is shown how component-level ESD testing and transient simulations (SPICE and mixed-mode) enable an efficient and reliable system-level ESD protection design.

Packaging Principles for the PrM (3 Hour) FC200

Certification: PrM

To provide clear-cut information on what type of controlled packaging should be used in any situation, EOS/ESD Association, Inc. released a comprehensive revision of the obsolete industry standard EIA 541-1988. The newer document, ANSI/ESD S541, is the focus of this inclusive session. It provides information and guidance, as well as material specifications, to assist in the design and implementation of a packaging plan for use within an ANSI/ESD S20.20 based ESD control program. Current and newly released test method standards suitable for packaging material evaluation will be described. Course credit applies to the ESD program manager certification curriculum. Previous attendance at the " FC100: ESD Basics" and "FC101: How To's" tutorials are highly recommended.

Practical Aspects of Latch-Up for Low Voltage CMOS: Design Rules, Layout Floor Planning, and Test (1 Hour) DD222

The idea of this tutorial would be to tackle the practical aspects of designing and testing for latch-up robustness. From a design perspective, layout floor-planning, design rules, and EDA checks will be covered. From a test perspective, standard DC latch-up testing as well as transient latch-up testing (including system-level ESD, cable discharge, and the evolving transient latch-up standard) will be covered. Finally, real world latch-up failures and diagnoses will be presented.

Quantifying System Level ESD and Protecting I/O (3 Hours) IEDS21-2

This seminar will describe the different entry paths of ESD into a system, such as the breakdown through gaps in the plastic, the corona induced currents from discharges to displays, and the discharges into I/O such as USB. This will enable engineers to quantify the threat for the different entry paths, and base design guidelines on this information. In the second, part this seminar will explain the System Efficient ESD Design strategy that allows to design efficient protection even for 10 GHz+ I/O based on simulation. The simulation needs transient models for the TVS diodes and models for the ICs. It is shown how these models are obtained and how the simulation is performed. The last part of the seminar will show how to even reduce the likelihood of soft-failure on I/O, such as USB by selecting protection elements based on simulation.

Safe Equipment Handling in Your EPA Explained (1 Hour) FC105

This class provides the essential knowledge required to safely handle sensitive items and set up and maintain an EPA. This course also gives service provider organizations that may not have formal quality management systems (QMS) training to ensure you have the necessary understanding to handle properly and repair client equipment, including a personal cell phone. Some cell phone manufacturers have set requirements for service providers to show that they have controls in place to reduce risks associated with static electricity. This training gives electronic equipment manufacturers confidence to safely repair and refurbish equipment like laptop computers, servers, printers, cell phones, and other devices. This same training is useful for organizations as they handle their own sensitive equipment or parts in their EPA.

SoC ESD Design and Verification (3 Hours) IF21-3

This tutorial fosters thinking and development of the appropriate design/verification for a situation by discussing the design environment and fundamentals and verification fundamentals. Key aspects of SoC ESD design and verification are often greatly misunderstood. The effects of these misunderstandings on ESD design are reviewed. Case studies are explored to help inform both the design and verification process.

Susceptibility Testing of Devices and Systems (1 Hour) DD/FC 132

There is a disconnect in the EMC (Electro Magnetic Compatibility) world between system manufacturers testing systems for upset and device manufacturers testing devices for failure. Some system level manufacturers are pushing device manufacturers to test semiconductor devices using system level compliance standards – specifically, IEC 61000-4-2 for ESD (Electrostatic Discharge). Product manufacturers would like to believe that if devices are qualified to IEC standard(s); finished products will likewise be qualified. Unfortunately, there is a fundamental difference between system level and device level testing; fortunately however, this difference can be bridged using new susceptibility scanning techniques on the board or device. Until now, EMC and ESD susceptibility testing at the device level has not been done. In this course, we will cover scanning methods (using a magnetic field noise source and probe) that allow identification of susceptible devices in a system, sensitive areas/pins of devices and associated circuitry.

System Level ESD & EMC Design (3 Hours) IF21-1

This tutorial provides an understanding of system-level ESD exposure. The IC/PCB co-design approach for (external) IC pins is discussed. Additionally, system efficient ESD design (SEED) opportunities and constraints are explored.

System Level ESD/EMI: Principles, Design Troubleshooting, & Demonstrations (3 Hours) DD/FC240

System level ESD tutorial about how to reduce ESD effects on systems (boards, chassis, etc.). Real circuits will be demonstrated in class showing techniques to correct the detrimental effects. Theory and real-life examples from recent past will be used to substantiate the methods.

Learning Outcome

- Understand how an ESD soft failure can upset a system and how to design to eliminate soft ESD failures
- Realize how ESD and electrical noise can enter a system and acquire methods to locate / remove the issues from ESD and electrical noise based on electric & magnetic field edification
- Encounter new methods to make a circuit board design more robust against direct ESD hits to a connector pin
- Assess the Faraday Shield principle and learn to apply it directly to applications in order to reduce detrimental ESD/EMI effects

System Level ESD/EMI: Testing to IEC and Other Standards (3 Hours) DD/FC130

Certification: DD

This tutorial is intended to help those tasked with testing products to system level ESD standards by providing first an overview of how real-world system ESD events are simulated in different standards and testers in general, and then provide detailed information on IEC 61000-4-2, the most widely used standard. This introduction will highlight the similarities and differences between IEC, ANSI, Telcordia, and some automotive ESD standards. We will answer common questions regarding test setups, test points, and procedures, and address key issues, including:

- Differences between “verification” and “calibration” and when is each required.
- Test equipment requirements, the test environment, ground connections, return paths, and ground plane effects.
- Testing procedures with demonstration on actual products, how the tester and procedure affects test results, and problems with test result variations due to simulator influences.
- Definitions of testing failure criteria for the product.
- What points need to be tested and why, guidance on determining “operator accessible” points and ports, exempted points and ports, and what to do around connectors and connector pins.
- ANSI and other ESD standards, the drive toward harmonization with IEC, the scope of different standards, and why they are unlikely to converge. This system level ESD tutorial will cover different perspectives on ESD as applied to electronic systems from the user’s, the designer’s, and even the designer’s competitor’s points of view.

System Level for the Program Manager (3 Hour) FC140

Certification: PrM

This tutorial is intended to help those tasked with testing products to IEC and other system level ESD standards by providing detailed information on IEC 61000-4-2, the most widely used standard, and highlighting the harmonization and differences among IEC, ANSI, Telcordia, and some automotive ESD standards. We will answer common questions regarding test set-ups, test points, and procedures, and address key issues, including:

- Differences between “verification” and “calibration” and when is each required; the influence of ESDA WG14 technical report (TR) on IEC and how it affects the calibration and verification procedures.
- Test set-up requirements, the test environment, ground connections, and return paths and ground plane effects.
- Testing procedures with demonstration on actual products, how the tester affects test results, and problems with test result variations due to simulator influences.
- What points need to be tested and why, guidance on determining “operator accessible” points and ports, exempted points and ports, and what to do around connectors and connector pins.
- ANSI and other ESD standards, the drive toward harmonization with IEC, why standards will probably never be the same as IEC, and the scope of different standards. This system level ESD tutorial will cover several facets of ESD as applied to electronic systems.

TCAD Fundamentals (1 Hour) DD117

Technology computer-aided design (TCAD) tools have become an indispensable utensil for the semiconductor industry. The possibilities to analyze, predict and optimize a certain semiconductor device behavior through modeling semiconductor fabrication (process TCAD) and semiconductor device operation (device TCAD) are countless. This includes the area for ESD and latch-up development. Early access to fundamental device parameters under very high current density and high temperature transients is the key to overcoming the conceptual problem of concurrent engineering for ESD engineers.

This tutorial serves as a basic introduction to the TCAD toolchain, including process and device simulation and the creation and integration of compact models for mixed more simulation. Focus points are the capabilities and limitations of these tools, like the requirements for a 2D/3D simulation approach and the validity of the models describing the fundamental physics, especially in the high-temperature regime.

Learning Outcome

On the one hand the tutorial is aimed at ESD and latch-up experts who want to clarify for themselves or their environment to what extent the use of TCAD is worthwhile in their development environment and how an introduction can be designed. On the other hand, the tutorial is interesting for students who deal with device physical effects such as high current injection and high temperature as part of their work. At the end of the course participants will have basic knowledge about the TCAD world including process and device simulation. Here the focus points are the capabilities but also limitations of these tools, like the requirements for a 2D/3D simulation approach and the validity of the models describing the fundamental physics, especially in the high temperature regime. The newly worked out second part sheds a light on selected applications allowing to understand what kind of typical ESD related questions can be addressed by such alternate development and analysis technique and what is the typical approach to get reasonable answers by the simulation tools. This part is also accompanied by a “Live-demo” that helps the interested audience to get an even more real(istic) insight into the whole tool chain and its application.

TCAD Methodologies for Industrial ESD Design (1 Hour) DD205

This seminar provides a comprehensive overview of the TCAD methodologies and best practices for industrial ESD design. Both the generic simulation workflow review and the classification of the most representative cases are covered. The advanced capability of mixed-mode simulation approach with device, circuit and process parameterization is demonstrated. Fabless and fab-light industry trends are addressed by overcoming the critical requirement of the well calibrated process simulation flow. The overall goal of the seminar is to add a new dimension to the standard R&D methodology and make it directly useful to a broad audience of ESD device, circuit and application engineers rather than corporate TCAD experts.

Tech Needs for ESD Enablement : Impact of Technology Parameters, Technology Scaling vs ESD Design (3 Hours) IF21-5

This tutorial gives students an understanding of the physics of basic components under high current conditions with a particular emphasis on scaling aspects. Additional information describes how to design components to meet a given target optimally. Specific challenges in HV ESD design, especially intrinsic power scalability, are reviewed. The primary focus is on technologies above 32 nm rather than sub-32 nm technologies.

TLP Fundamentals – Understanding the Equipment Options (1 Hour) DT210

Certification: DT, EDEC

This tutorial will explain what Transmission Line Pulsing (TLP) is and how it can be used for ESD design and development. Taking accurate TLP measurements is important thus how TLP systems make measurements and produce IV plots will be reviewed. The IV plots provide very valuable device parameters that are key to understanding the DUT being stressed. The tutorial will also explain the parameters that can be extracted from those IV curves. Finally typical equipment used in TLP systems will be reviewed.

Towards Optimal ESD Protection Diodes in AAdvanced Bulk FinFET and GAA Technologies (1 Hour) IEDS21-3

Transmission Line Pulse (TLP) Basics and Applications (3 Hours) DD220

Certification: DD

This tutorial will cover the basics of TLP including underlying theory, the types of TLP systems available, and how I-V curves are extracted from TLP pulses. The tutorial uses examples to show how fundamental device parameters can be measured with TLP. These parameters allow the ESD engineer to understand a technology's properties which can be used to design successful ESD protection circuits. The student will gain an understanding of the purpose of TLP measurements, how TLP relates to HBM and CDM, fundamentals of how TLP systems work, including impedance and refl ections, types of TLP systems, importance of load lines, adaptive ranging, TLP calibration, time dependence from TLP, and biased TLP measurements. The tutorial will present examples of TLP use for nMOS transistors, diodes, oxides/capacitors, and power supply clamps, as well as time dependent TDR-O and VF-TLP examples.

Ultra-Sensitivity Trends and CDM (1 Hour) GP241

The electronics industry faces a double challenge: increasing use of ultra-sensitive devices and lack of experience with the Charge Device Model (CDM). This class will give you the background to understand the challenges and prepare to meet them. Case studies will illustrate how CDM failures can persist even with a robust HBM program in place. A series of photographs of common CDM issues in manufacturing will enable students to visualize how to implement CDM controls. A brief summary of the work by the Industry Council on ESD Target Levels will be included.

Ultra-sensitive (Class 0) Devices: ESD Controls and Auditing Measurements (3 Hours) FC361

Advanced ESD controls and auditing measurements for CDM & Class 0 (ultra-sensitive) devices and circuit boards are not well known and there are many technical and strategic pitfalls that must be avoided. Industry definitions (threshold levels) for Class 0 will be described and the history of their use will be reviewed. The Class 0 category is broken down into sub-categories of increasing risk. Students will learn how to make valid measurements, avoid common pitfalls, and how to use this data to successfully handle Class 0 sensitivities. Advanced measurements will be described including event detection and high speed current measurements. Students will learn when each measurement type is useful. Compelling case studies will illustrate these techniques and the success they produce.

ESD Control procedures for Class 0 manufacturing require customization, attention to detail and a full understanding of the technology. Thus, each company will need to develop a Class 0 ESD subject matter expert (SME) to ensure the correct and cost effective counter measures are taken. SOPs (special operating procedures) developed by SMEs will be discussed that have proven to virtually eliminate Class 0 failures.

This tutorial will be highly interactive with live demonstrations, in-plant photographs, and video clips. Students will be encouraged to ask questions and actively participate in the discussions. References to technical literature on ultra-sensitive devices will be included.

Use of the Digital Sampling Oscilloscope for ESD Measurements (3 Hours) DD/FC122

The digital sampling oscilloscope (DSO) finds application in measuring waveforms that occur infrequently or only once. Its sophisticated calculation and display capabilities give it utility for factory ESD, as well as, its role in monitoring ESD immunity waveforms for both component and system level ESD. Understanding instrument performance issues is important for proper use. DSO bandwidth and the sampling rate are often used interchangeably, although they serve completely different purposes. The bandwidth, sampling rate and memory depth of the instrument must be specified for the intended application. DSOs also have display modes which can hide undersampling artifacts and lead to incorrect conclusions. Selecting the appropriate display algorithm is important for both cosmetic purposes and to achieve correct results from the instrument. Also important for the proper use of any oscilloscope are selection of the input impedance and the setup of the trigger. For a DSO, the pretrigger value must also be set. In some cases equivalent time sampling can be used but in most ESD measurements, single shot acquisition is required. Finally, for ESD applications on the factory floor, there are a variety of probes that are used. These include, wide bandwidth current probes, clamp on current probes, single ended and differential voltage probes, as well as, high frequency antennas.

VF-TLP, An Introduction to Capabilities and Applications (1 Hour) DT212

Certification: DT

VF-TLP stands for Very Fast Transmission Line Pulsing. Standard TLP uses typically 100 ns long pulses. It allows the device characterization in the HBM time domain. VF-TLP uses pulses with a duration of a few nanoseconds and faster rise times than standard TLP. It allows the device characterization and (transient) voltage and current measurement in the CDM time domain. This tutorial explains the VF-TLP measurement setups, equipment options and how the extracted data is interpreted. Several examples explained how the VF-TLP setup parasitic are de-embedded and applied to the obtained “raw” measurement data. The goal of the tutorial is to enable the operator to deliver high quality measurement data to the ESD protection designer.