2024 International ESD Workshop (IEW) – Asian In-Person Event

Annual International Electrostatic Discharge Workshop

July 15-18, 2024 Marina Bay Sands Expo and Convention Centre Singapore

CALL FOR POSTERS

In July, 2024, we will embrace brand new IEW-Asia event co-located with the International Physical and Failure Analysis of Integrated Circuits (IPFA2024). Never change, IEW will continue to provide a relaxed, invigorating atmosphere to present new work and engage in discussions about the latest issues confronting the ESD and EOS communities in its 17th year. The workshop will retain the peculiar elements: a tutorial, invited seminar speakers, discussion groups, invited talk speakers, technical presentation sessions, and special interest groups. In addition to everything IEW-Asia provides, IEW-Asia registrants will also be able to attend the full IPFA technical program (any technical session, invited talks, and keynote speakers), including the joint evening poster reception showcasing works from both conferences. IPFA registrants will have access to IEW keynote and invited talks (but not the other unique elements of IEW-Asia). **Therefore, submissions to IEW-Asia will receive exposure to a much broader audience.**The IEW is the perfect opportunity to submit late-breaking and exciting new research to stimulate discussion and interaction around new ideas, encouraging new research topics, as shown below:

FOCUS TOPICS FOR IEW 2024

Automotive Applications ESD/EMC

The electronic content of automobiles is increasing, leading to more complex electronic modules and system design. Integration of ICs and discrete devices are demanding, considering the module-level EMC testing and reliability requirements. The IEW invites contributions that address ESD and EMC challenges in automotive systems design, including complying with standards such as bulk current injection (BCI), direct power injection (DPI), IEC-61000-4-2, ISO-10605, and ISO-7637.

2.5D/3D hetero-Integrations

System-Technology Co-Optimizations (STCO) with 2.5D/3D hetero-integrations and chiplet design concepts have been considered as a major future innovation booster in semiconductor and electronics industry. The IEW invites on-going research and development work to better understand the ESD effects during the 2.5D/3D hetero-integrations? Your research and development work can provide guidance on ESD target levels, on ESD testing of die-to-die interfaces and for IP development in 2.5D and 3D ICs.

Failure Analysis Techniques

Locating failure sites, particularly for CDM, imaging techniques, correlating FA-identified damage sites with ESD stress, distinguishing EOS-like failures from ESD failures, and unusual failure modes. The IEW invites contributions that address recent FA techniques to improve the understanding of corresponding failure mechanisms.

New Developments in Latch-Up

Emerging product trends such as technology scaling (e.g., FinFET versus planar CMOS), increasing product complexity, and more demanding operation environments (e.g., automotive; high junction temperature; radiation-induced latch-up; etc.) all lead to the stark reality that latch-up will be a major reliability threat for the foreseeable future. The IEW welcomes you to share your experience and perspective on this important topic.

Electrical Overstress (EOS)

EOS continues to be one of the semiconductor industry's largest causes of customer returns. Have you recently completed root-cause analysis on a failure with an electrical induced physical damage (EIPD) signature? There is no

defined procedure to determine a product's absolute maximum ratings (AMR). Do you have a methodology for defining AMR for a product and verifying it for different timescales? Are you an FA engineer with experience in case studies identifying EOS damage mechanisms and the ensuing physical evidence? Do you have experience auditing a manufacturing site for sources of EOS? Bring your work to the IEW and share it with your colleagues.

Other topics and areas to consider for abstract submissions include but are not limited to:

Anomalous/Unresolved ESD Issues

Random and unrepeatable ESD failures, case histories, ESD tester correlation issues, and unique window failures.

System ESD

Cable Discharge Event (CDE): test methods, applicability, design impact, potential standardization. System ESD design: co-design between the system board and the component (SEED). System ESD simulation methods and component modeling, new stress models. On-chip design methods for improving system ESD. System ESD-related failure modes and case studies. Test methods for validating ESD on the board level: is test standardization of component robustness under system ESD feasible?

ESD Big Data

Summarize and view large ESD and latch-up tester datasets, view CDM waveform parameter statistics, and map design data to ESD and latch-up test programs.

EDA Tools

EDA verification and simulation tools; techniques, design flows, best practices, experiences with foundry rule decks, commercial tools, and custom tooling.

ESD Control

As technologies continue to change, we need to consider the control methods being used and continually review the standards and methodologies being used to ensure the best practices are being followed. Case in point, to provide the industry with the best standards possible, ANSI/ESD S20.20/JESD 625B working groups are looking at harmonizing these documents. We also need to consider whether there are any weak points in today's processes that may require updates to the control standards or new standards to cover new technologies. The use of discharge detectors as a tool for analyzing problem areas within assembly has proven to be very useful. Should analysis tools like discharge detectors become standard in the Control process?

Novel On-Chip Protection Clamps and Circuit Configurations

New clamp devices and clamp configurations, methods to increase the failure threshold of protected devices, high voltage clamps for automotive and power amplifiers, new chip protection concepts, and low-capacitance clamps for RF and high-speed interfaces.

ESD Test Characterization, Methods, and Issues

TLP & VF-TLP debug and device characterization methods, correlation of TLP & VF-TLP tests with standard qualification tests, HBM and CDM tester artifacts, unresolved test results and failures, issues relating test qualification levels to real-world exposure, test chip methodology, cable discharge test methods, and test standards issues.

Technology Integration Issues

ESD sensitivity with technology transfers, 2.5D/3D IC ESD design issues, qualification challenges for different fabs, unusual problems of process interaction with ESD, process monitor methods, and technology scaling issues.

IMPORTANT DATES

18th March, 2024
Abstract Poster Submission Deadline

22nd April, 2024
Notification of Acceptance

1st July, 2024
Final Poster Due

Submission Guidelines

Thanks to the co-location with IPFA, submissions will occur through the IPFA website (https://ipfa-ieee.org/2024/call-for-papers-2024/). Submission instructions and an abstract template are available at IPFA website and https://www.esda.org/events/2024-asia-esd-workshop-asia-iew-co-located-with-ipfa-2024. The submission is in PowerPoint format and is no longer than 6 slides. Submissions are due 18th March, 2024. There will be no published proceedings of IEW. Walk-on posters are also permitted at IEW with no prior review, but only those works which are submitted for review and acceptance will be included in the five-minute teaser presentation sessions.